Ultra-low thermal budget, BEOL-compatible, correlated electron random access memory (CeRAM) for harsh environment applications

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The future of monolithic 3D integration relies on low-temperature, back-end-of-line (BEOL) compatible electronic devices. Si-based logic and memory technologies rely on extremely high temperature (> 800 °C) anneal for doping activation and contact formation. We need technologies that can be made within the typical BEOL thermal budget of 450 °C for 1 hour without losing the performance.

This abstract demonstrates an ultra-low temperature process (< 450 °C) for a novel, non-volatile memory technology based on correlated electron materials known as CeRAM [1]. Even with a low thermal budget, the novel physics in CeRAM can successfully operate from <-272 °C to > 300°C [2, 3]. Carbon doping of transition metal oxides enables correlated electron physics, which enables bulk-like, solid-state resistance change in the application of electrical pulses. CeRAM, unlike other resistive switching memories, does not rely on filament formation or defect migration for resistive switching. Carbon doping also has the secondary benefit of effectively neutralizing oxygen vacancies, making the film robust against filament formation. Lower defects significantly reduce variability and improve reliability compared to other defect-drive, resistive switching memories.

This work outlines challenges in achieving a uniform, carbon-doped film at low thermal budgets. We will also discuss the role of carbon doping in achieving CeRAM. This abstract will also discuss the optimization of CeRAM films by utilizing two deposition techniques (Spin Coating and Physical Vapor Deposition), grain and crystallite distribution, thickness, and morphology changes. We perform detailed characterization using SEM, AFM, XRD, XPS, HRTEM, and in-situ HRTEM to understand the crystallite evolution in CeRAM operation.

This project is an example of successfully traversing the lab-to-fab gap in early-stage semiconductor development. We have further optimized micron-scale devices to sub-500 nm CeRAM devices and improved the power and reliability. The scaled devices' performance will be discussed with unique harsh environment applications such as quantum computing and NASA's Venus probe mission that could be served with CeRAM non-volatile memory.

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References

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